Notice of Allowability	Application No.	Applicant(s)	
	10/721,096	NAKAMORI ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 1/31/05*.

2. ☒ The allowed claim(s) is/are *11-14 and 16-20*.

3. ☒ The drawings filed on *27 September 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

1. Claims 11-14 and 16-20 are allowed.

2. The following is an examiner's statement of reasons for allowance: a current supply circuit supplies a bias current to operational converter having a current switching circuit which switches between output currents in response a control means, thereby switching between currents to be supplied from a bias circuit to the operational amplifiers via transistors. A sufficiently large current enough for the to a current control signal from current amplifiers to operate at a high frequency is supplied, while amplifiers which constitute a pipelined AD the current is switched to a lower supply current for the amplifier to operate at lower frequencies. This bias control circuit for op amps has not been shown in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Leifso, et al 6,870,425 disclose a gain control circuit that permits a variable gain amplifier circuit to operate with high input linearity and low power consumption is disclosed. The variable gain amplifier includes a standard differential bipolar transistor input circuit and a pair of degeneration transistors connected to a current source transistor. The gain control circuit provides a variable degeneration control voltage to vary the effective resistance of the degeneration transistors and a variable bias voltage to vary the current of the current source transistor. The input

linearity of the variable gain amplifier is controlled independently of gain by adjusting the effective resistance and the current in an inverse relationship such that at maximum gain the current is at a maximum while the degeneration resistance is at a minimum, and at minimum gain the current is at a minimum while the degeneration resistance is at a maximum. Therefore the variable gain amplifier can be controlled to operate with high input linearity and low power at lower ranges of gain.

Pehike 6,765,443 discloses a bias controller that sets the quiescent current of a power amplifier to a desired value by dynamically adjusting the power amplifier bias voltage. Using closed-loop control, the bias controller sets the bias voltage to whatever value is needed despite circuit component variations and temperature effects. Operation of the bias controller complements dynamic bias voltage adjustment in advance of transmit operations, such as in advance of a transmit burst. In a first state, where the power amplifier is in a quiescent condition, the bias controller adjusts bias voltage to set the desired quiescent current by detecting the supply current into the power amplifier. The bias controller then transitions to a second state, where it maintains the adjusted bias voltage irrespective of amplifier supply current. Despite its ability to sense supply current into the power amplifier, the bias controller's configurations avoid dissipative current sensing during normal operation of the power amplifier.

Arell, et al 6,753,734 disclose a bias circuit exhibiting good stability over variations in temperature and power supply voltage and capable of generating a plurality of discrete levels of output current for biasing RF power amplifier. In accordance with the invention,

the bias circuit includes (1) a master transistor connected to the slave transistor in a current-mirror configuration and having two parallel-connected transistor elements, (2) a switch connected to at least one transistor element to control its operation, and (3) a feedback circuit by which the voltage at the collector of the master transistor may be fed back to control the voltages at the bases of the master transistor and the slave transistor.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819